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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,777	03/04/2004	Michikazu Matsumoto	60188-793	4422

7590 11/17/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,777	MATSUMOTO, MICHIKAZU	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *30days* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *19-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-18* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This restriction is in response to the election filed August 29, 2005.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species of the claimed invention:

Embodiment I (Claims 1 and 3), directed to a MOS transistor, a dummy pattern wherein the dummy pattern is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode and first and second silicide layers;

Embodiment II (Claims 1, 4 and 6), directed to a MOS transistor, a dummy pattern wherein the dummy pattern is made of an insulating layer and first and second silicide layers;

Embodiment III (Claims 1 and 5), directed to a MOS transistor, a dummy pattern is either a pattern made of an insulating material or a dummy gate electrode which is an electrode pattern and is not electrically connected to a semiconductor integrated circuit and first and second silicide layers;

Embodiment IV (Claims 1 and 7-10), directed to a MOS transistor, a dummy pattern wherein the dummy pattern is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode and first and second silicide layers wherein the MOS transistor is formed in an element region surrounded with an isolation insulating film and the pattern made of insulating material is formed on the isolation insulating film;

Embodiment V (Claims 1 and 11-13), directed to a MOS transistor, a dummy pattern wherein the dummy pattern is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode and first and second silicide layers wherein the gate electrode comprises two portions extending substantially parallel to each other and a connecting portion respective ends of the two portions to each other;

Embodiment VI (Claims 2 and 3), directed to a MOS transistor, a plurality of gat electrodes wherein each gate electrode is arranged between the other gate electrodes or between one of the gate electrodes and a dummy pattern with a space left at each side thereof and first and second silicide layers;

Embodiment VII (Claims 2, 4 and 6), directed to a MOS transistor, a plurality of gate electrodes wherein each gate electrode is arranged between the other gate electrodes or between one of the gate electrodes and a dummy pattern with a space left at each side thereof wherein the dummy pattern is made of an insulating layer and first and second silicide layers;

Embodiment VIII (Claims 2 and 5), directed to a MOS transistor, a plurality of gat electrodes wherein each gate electrode is arranged between the other gate electrodes or between one of the gate electrodes and a dummy pattern with a space left at each side thereof and first and second silicide layers, a dummy pattern is either a pattern made of an insulating material or a dummy gate electrode which is an electrode pattern and is not electrically connected to a semiconductor integrated circuit and first and second silicide layers;

Embodiment IX (Claims 2 and 7-10), directed to a MOS transistor, a plurality of gat electrodes wherein each gate electrode is arranged between the other gate electrodes or between one of the gate electrodes and a dummy pattern with a space left at each side thereof and first and second silicide layers wherein the MOS transistor is formed in an element region surround with an isolation insulating film and the pattern made of insulating material is formed on the isolation insulating film;

Embodiment X (Claims 2 and 11-13), directed to a MOS transistor, a plurality of gat electrodes wherein each gate electrode is arranged between the other gate electrodes or between one of the gate electrodes and a dummy pattern with a space left at each side thereof and first and second silicide layers wherein the gate electrode comprises two portions extending substantially parallel to each other and a connecting portion respective ends of the two portions to each other;

Embodiment XI (Claims 14 and 15), directed to a MOS transistor, the gate electrodes are formed on a semiconductor substrate having a silicon layer, each of the gate electrodes is arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern with a space left from each side thereof, sidewalls and a first and second silicide layer wherein the dummy pattern is a dummy gat electrode which is an electrode having the shape of a gate electrode;

Embodiment XII (Claims 14 and 16), directed to a MOS transistor, the gate electrodes are formed on a semiconductor substrate having a silicon layer, each of

the gate electrodes is arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern with a space left from each side thereof wherein the dummy pattern is made of insulating material, sidewalls and a first and second silicide layer;

Embodiment XIII (Claims 14 and 17), directed to a MOS transistor, the gate electrodes are formed on a semiconductor substrate having a silicon layer, each of the gate electrodes is arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern with a space left from each side thereof wherein a dummy pattern is either a pattern made of an insulating material or a dummy gate electrode which is an electrode pattern and is not electrically connected to a semiconductor integrated circuit, sidewalls and a first and second silicide layer; and

Embodiment XIV (Claims 14 and 18), directed to a MOS transistor, the gate electrodes are formed on a semiconductor substrate having a silicon layer, each of the gate electrodes is arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern with a space left from each side thereof wherein the pattern made of insulating , sidewalls and a first and second silicide layer.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claim 1 is generic to claims 3-13, claim 2 is generic to claims 3-13 and claim 14 is generic to claims 15-18.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee under 37 CFR 1.17(i).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

November 5, 2005